REMARKS

Please cancel Claims 6, 11 and 15 without prejudice. Claims 1-4, 7-8, 12-13, 16-21 and 23 are pending. Claims 1, 4, 7 and 16 are amended herein. No new matter is added by the claim amendments. Support for the claim amendments can be found at least on page 13 (lines 7-11) and page 14 (lines 11-13) of the instant application.

Drawings

According to the instant Office Action, the drawings are objected to because Figure 3 fails to show any of the detail of circuit 320. The instant specification refers to "device 320," which is described as being implemented in a number of different ways, such as a resistor or transistor. According to 37 CFR § 1.83, conventional features (which presumably include a resistor or transistor) can be illustrated in the form of a labeled representation (e.g., a labeled rectangular box). Applicant respectfully submits that Figure 3 (specifically, device 320) satisfies this requirement. Accordingly, Applicant respectfully submits that Figure 3 does not require corrective action.

35 U.S.C. § 102 Rejections

According to the instant Office Action, Claims 1-4, 7-8, 12-13 and 16-21 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kadanka et al. ("Kadanka;" U.S. Patent No. 5,621,308). The Applicant has reviewed the cited reference and respectfully submits that the present invention as recited in Claims 1-4, 7-8, 12-13 and 16-21 is neither anticipated nor rendered obvious by Kadanka.

According to the Federal Circuit, "[a]nticipation requires the disclosure in a single prior art reference of each claim under consideration" (W.L. Gore & Assocs. v. Garlock Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983)). However, it is not sufficient

that the reference recites all the claimed elements. As stated by the Federal Circuit, the prior art reference must disclose each element of the claimed invention "arranged as in the claim" (emphasis added; Lindermann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984)).

Applicant respectfully submits that Kadanka does not show or suggest the claimed circuit structure or the claimed functionality of the circuit in operation. Specifically, Applicant respectfully submits that Kadanka does not show or suggest "a band-gap reference unit comprising a plurality of transistors; ... and a second transistor operable as an emitter follower for the emitters of said plurality of transistors, wherein the emitter of said second transistor is electrically coupled to said buffer circuit via said voltage pull-up device, wherein said second transistor and said voltage pull-up device in combination pull the V_{BE} of said buffer circuit toward Vcc" as recited in independent Claim 1 and as similarly recited in independent Claims 7 and 16.

Accordingly, Applicant respectfully submits that Claims 1, 7 and 16 are in condition for allowance. Claims 2-4, 8, 12-13 and 17-21 depend from either Claim 1, 7 or 16 and recite additional limitations. Consequently, Applicant respectfully submits that Claims 2-4, 8, 12-13 and 17-21 are also in condition for allowance because they each depend on an allowable base claim.

In summary, Applicant respectfully asserts that the basis for rejecting Claims 1-4, 7-8, 12-13 and 16-21 under 35 U.S.C. § 102(b) is traversed.

35 U.S.C. § 103 Rejections

According to the instant Office Action, Claim 23 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Kadanka in view of Mietus (U.S. Patent No. 5,666,046). The Applicant has reviewed the cited references and respectfully submits that the present invention as recited in Claim 23 is neither anticipated nor rendered obvious by Kadanka and Mietus, either alone or in combination.

Claim 23 is dependent on Claim 16 and includes additional limitations. Hence, by demonstrating that Claim 16 is not shown or suggest by the combination of references cited, it is also demonstrated that Claim 23 is not shown or suggested by the combination of references.

As presented above, Applicant respectfully asserts that Claim 16 is not shown or suggested by Kadanka. Applicant respectfully submits that Mietus does not overcome the shortcomings of Kadanka. More specifically, Applicant respectfully submits that Mietus, alone or in combination with Kadanka, does not show or suggest "adjusting the voltage across said buffer circuit, by use of a voltage pull-up device in combination with a first transistor to pull the V_{BE} of said buffer circuit toward Vcc, wherein said voltage pull-up device is coupled between said buffer circuit and said band gap voltage reference unit, ... wherein said first transistor is coupled as an emitter follower for the emitters of said plurality of transistors, and wherein the emitter of said first transistor is electrically coupled to said buffer circuit via said voltage pull-up device" as recited in Claim 16. Applicant respectfully submits that Mietus, like Kadanka, does not show or suggest the claimed circuit structure or the claimed functionality of the circuit in operation as recited in Claim 16.

Accordingly, Applicant respectfully submits that Claim 16 is allowable over Kadanka and Mietus. Therefore, Applicant respectfully submits that Claim 23 is also in condition for allowance because it depends on an allowable base claim.

In summary, Applicant respectfully asserts that the basis for rejecting Claim 23 under 35 U.S.C. § 103(a) is traversed.

Conclusions

In light of the foregoing amendments and remarks, Applicant respectfully submits that Claims 1-4, 7-8, 12-13, 16-21 and 23 are in condition for allowance. Applicant respectfully requests allowance of the pending claims.

The Applicant has reviewed the reference cited but not relied upon and did not find this reference to show or suggest the present claimed invention: U.S. Patent No. 6,118,264.

The Examiner is invited to contact Applicant's undersigned representative if the Examiner believes such action would expedite resolution of the present application.

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Respectfully submitted,

William A. Zarbis
Reg. No. 46,120

MURABITO HAO & BARNES LLP
Two North Market Street, 3rd Floor
San Jose, California 95113
(408) 938-9060